CMOS RF Circuit (EWE 8065) 상

Prof. Ickhyun Song

Group 2:

김태영

김현석

Final report

Contents

1. Receiver 2

2. Transmitter 8

2.2 Up conversion mixer 11

3. Conclusion 14

4. Contribution 14

1. Receiver

Direct Sampling UWB (6-10.2 GHz) radar transceiver

System

The receiver composed of LNA, Mixer, and VCO circuits is designed as a UWB Direct Conversion Receiver with over 4.2GHz RF bandwidth. DCR has advantages of low power consumption and high degree of integration, but has a disadvantage of low reception sensitivity. A direct conversion X-Band receiver was designed to obtain the desired gain with low power and low noise and to design a receiver utilizing the advantages of a simple structure.

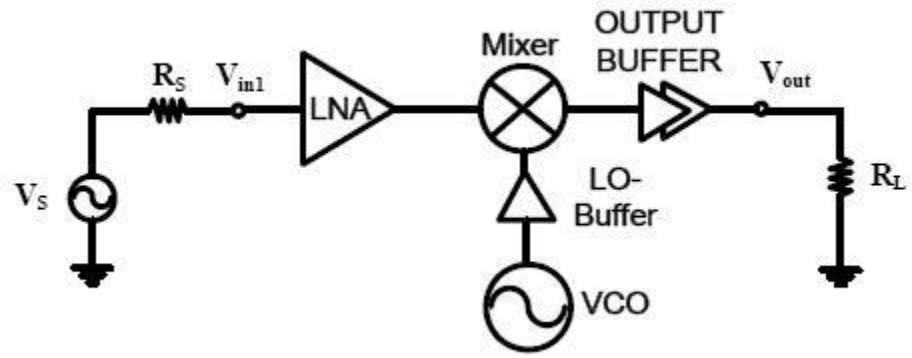


Figure 1. Top level receiver schematic

1.1 LNA(Low-Noise-Amplifier)

LNA, as the name suggests, is an amplifier designed to minimize noise.

An LNA takes a very weak, uncertain signal from an antenna and amplifies it to a more useful level. If noise is amplified in a very weak signal, the gain is greatly damaged and can have a great effect on operation. Therefore, LNA is an amplifier that can obtain gain while minimizing noise in this small signal. The LNA needs to check the noise figure (NF), gain and linearity. The LNA's power consumption and efficiency are not critical. First of all, the LNA does not consume large power due to its characteristics, and consumes more power in the next configuration. The proposed LNA utilizes a feedback structure to enable operation in a wide bandwidth.

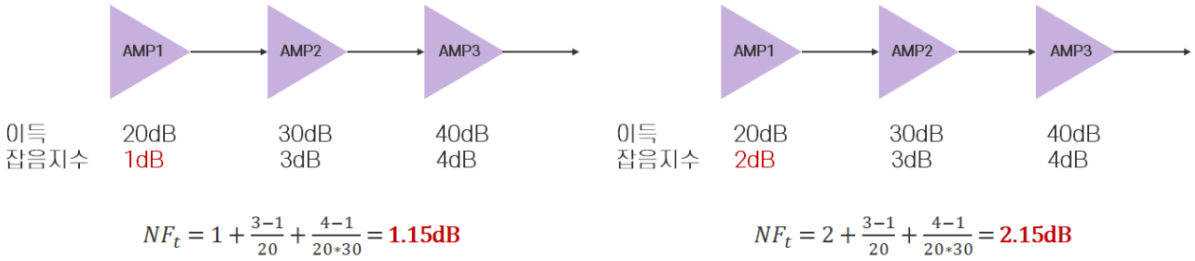
The reason why NF is important in the first stage is that the NF value is entered as it is in the first stage, and then multiplied by the amplification value of AMP, resulting in the following. Therefore, it is important to have low NF results in the first LNA.



$$NF_T = NF_1 + \frac{NF_2 - 1}{G_1} + \frac{NF_3 - 1}{G_1 G_2} + \cdots + \frac{NF_N - 1}{G_1 G_2 \cdots G_{N-1}}$$

NF_N : N번째 증폭기의 잡음 지수

G_N : N번째 증폭기의 증폭도



$NF_t = 1 + \frac{3-1}{20} + \frac{4-1}{20*30} = 1.15dB$

$NF_t = 2 + \frac{3-1}{20} + \frac{4-1}{20*30} = 2.15dB$

LNA used feedback as follows. Impedance matching is not wide due to the characteristics of CS-stage. Therefore, the UWB LNA was designed through the feedback structure.

Parameter	Value
V_{DD} (V)	1.8
Bias voltage (V)	0.73
Power (mW)	20.74
NF(dB)	3.13 ~ 5.09
Gain(dB)	14.5 ~ 15.42
S_{11} (dB)	< -9.34
S_{22} (dB)	< -12.66
P1dB (dBm)	-4.3
IIP_3 (dBm)	-4.787

Table 1. LNA 성능 파라미터

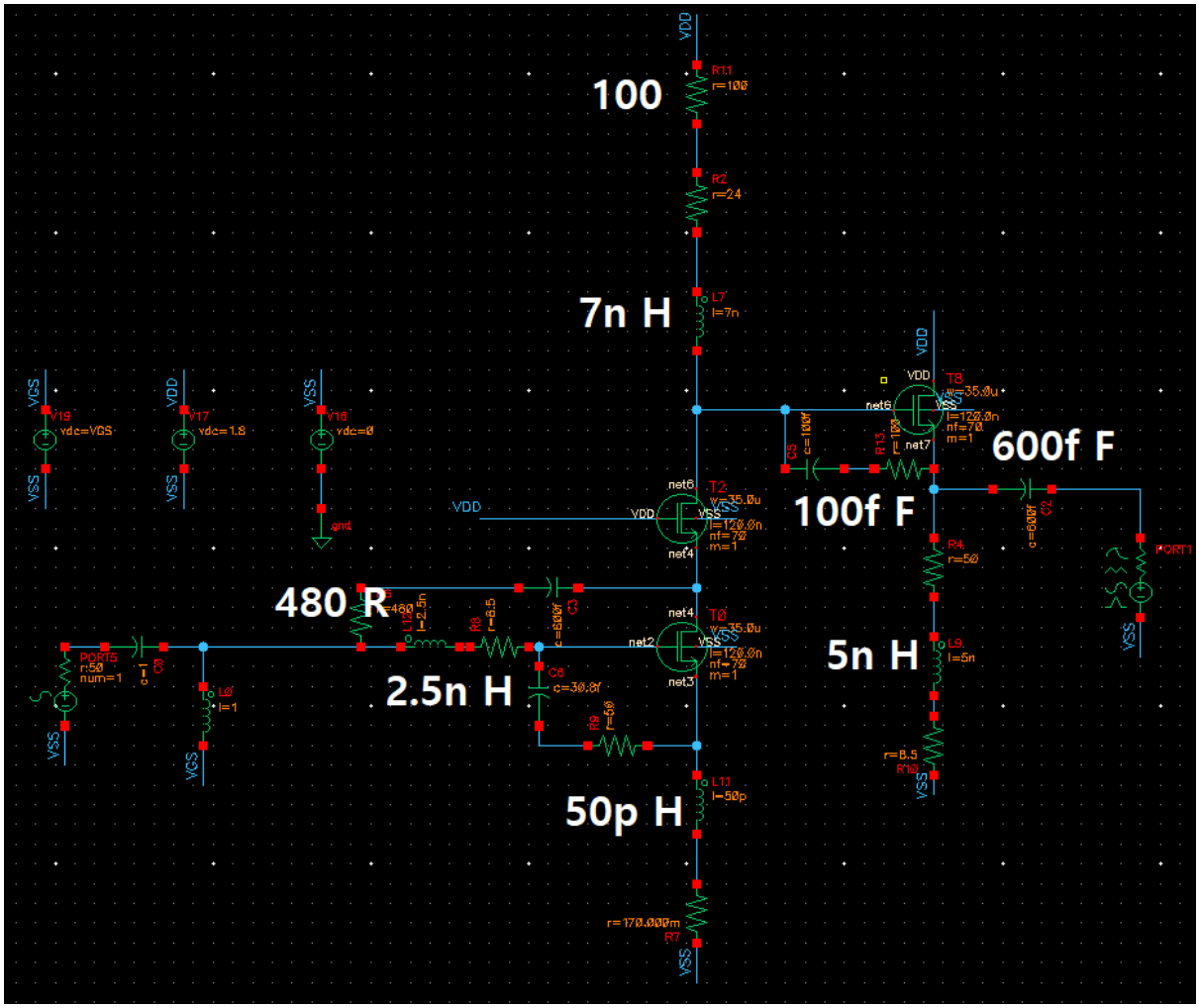


Figure 2. Proposed LNA Circuit

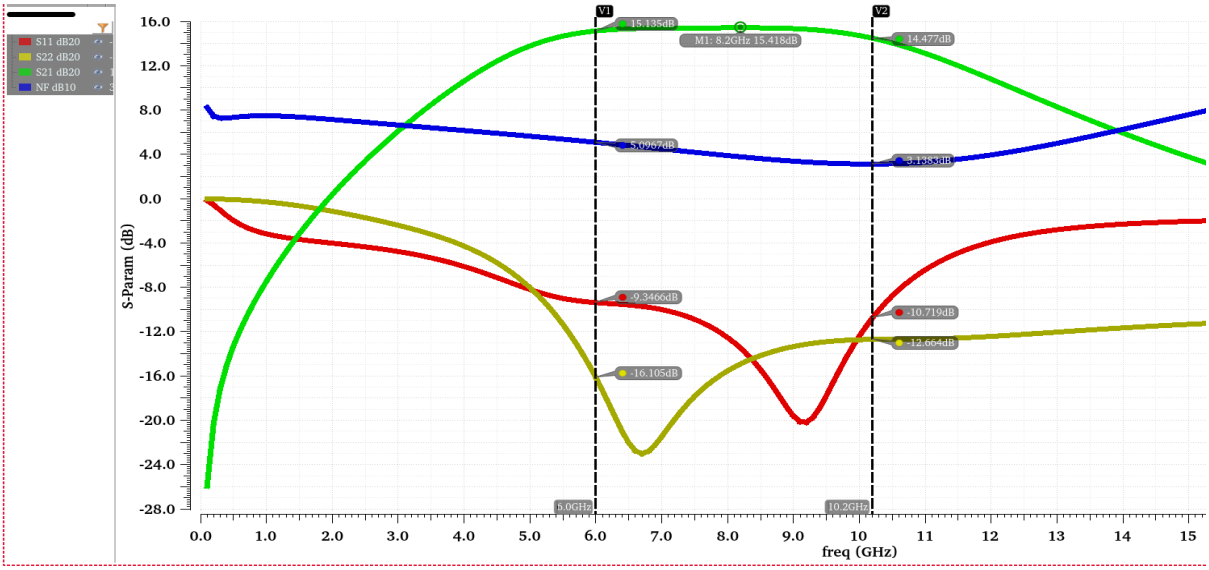


Figure 3. LNA S-parameter & Gain

1.2 VCO

In order to secure enough gm for oscillation, the VCO adopts a current-reuse LC VCO structure that can obtain high transconductance compared to current by using NMOS and PMOS together. The advantage of this structure is that it is easy to satisfy the Barkhausen criterion for oscillation even with an inductor with a low Q factor because high transconductance can be obtained. However, since the PMOS is added, the output voltage headroom is reduced.

Instead of adding a phase shifter to operate two I and Q signals in 90 degree phase in the receiver and transmitter, the VCO is designed as a quadratic LC VCO. Quadratic LC VCOs have about 5dB higher phase noise than differential LC VCOs.

The output buffer used a push-pull structure. It is designed so that the operating frequency does not change due to the output load through the output buffer.

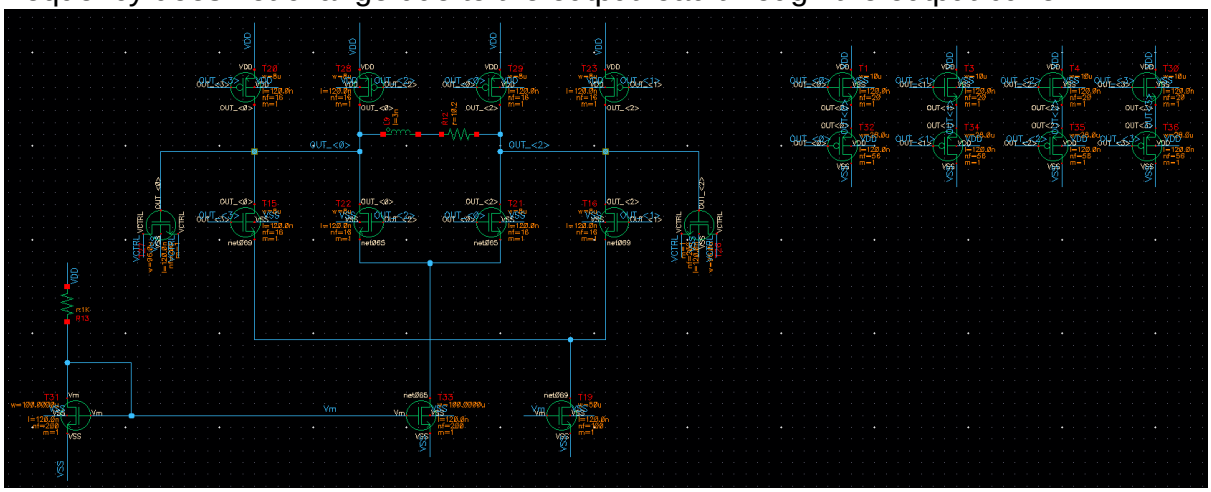


Figure 4. Proposed VCO Circuit

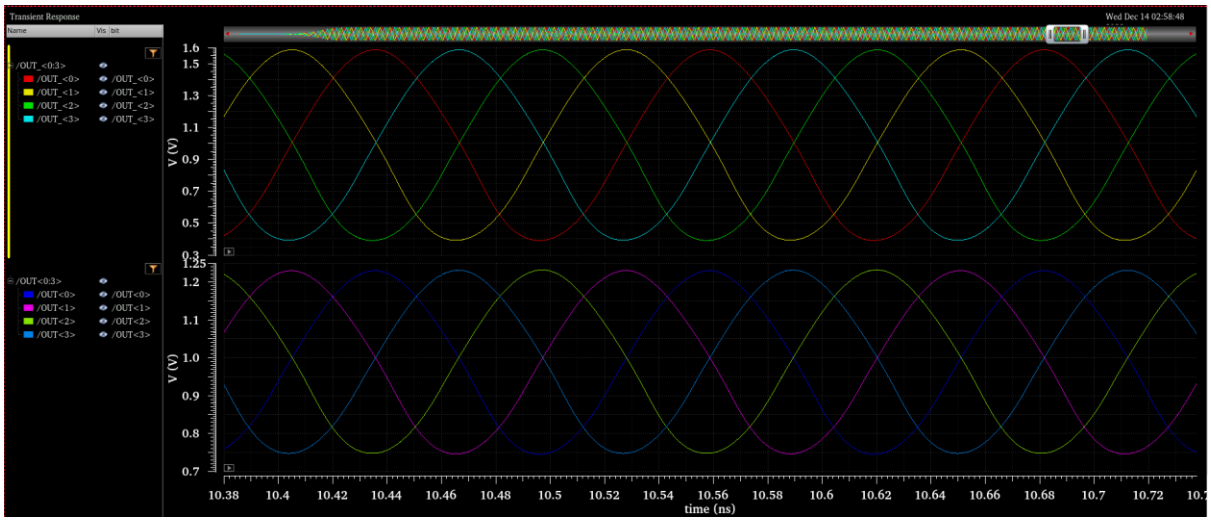


Figure 5. VCO Simulation

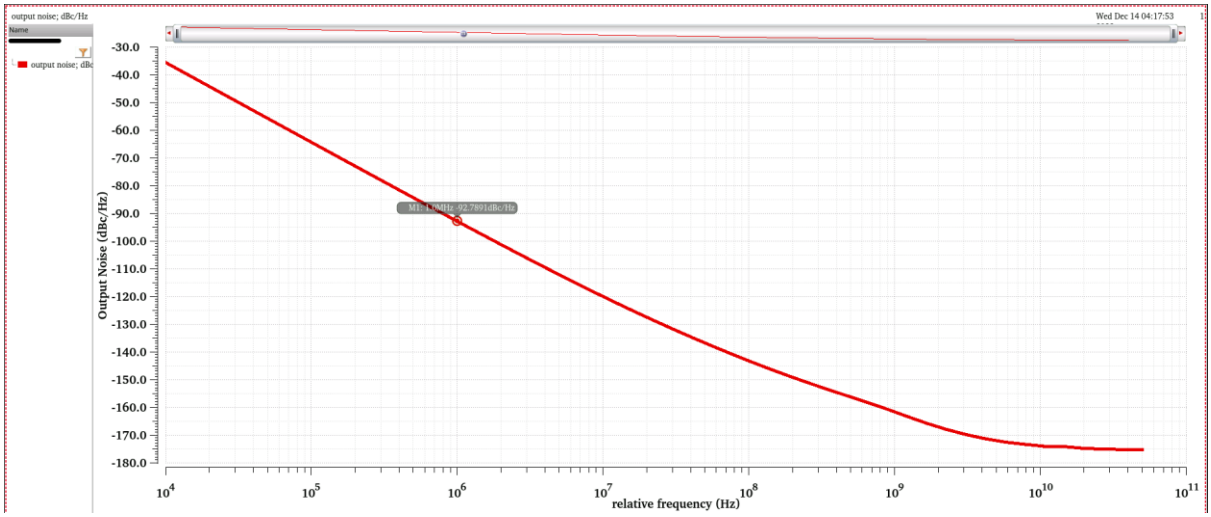


Figure 6. Phase Noise of VCO

Nr.	Tch., nm	Fc, GHz	ΔF, %	PN, dBc/Hz	PN@*df*, MHz	P, mW	FOMt, dBc/Hz
[5]	350	5.88	3.91	-112.00	1	19.20	-166.40
[6]	250	7.45	30.76	-100.00	1	0.54	-189.87
[7]	250	4.89	13.09	-124.00	1	22.00	-186.70
[8]	250	3.61	6.38	-130.70	1	22.60	-184.39
[9]	180	4.00	47.70	-115.60	1	2.99	-196.45
[10]	180	12.77	15.75	-110.20	1	1.08	-195.93
[11]	180	1.85	9.21	-126.00	1	1.35	-189.31
[12]	180	13.00	25.62	-101.40	1	2.40	-188.05
[13]	180	18.90	1.06	-129.30	1	10.00	-185.32
[14]	180	1.82	10.99	-127.00	1	6.30	-185.03
[15]	180	5.32	7.52	-122.00	1	13.50	-182.74
[16]	180	5.36	13.81	-127.00	3	18.00	-182.29
[17]	180	12.31	28.11	-108.00	0.1	50.00	-180.88
[18]	180	3.3	21.21	-91.00	1	5.04	-181.79
[19]	180	5.56	15.30	-105.83	1	5.60	-176.94
[20]	180	7.65	6.54	-108.30	1	4.90	-175.38
[21]	180	29.82	1.38	-104.10	1	2.30	-172.74
[22]	180	5.25	0.76	-117.62	1	1.05	-169.45
[23]	180	2.05	63.08	-83.82	1	11.20	-155.54
[24]	130	5.71	37.69	-132.68	1	2.21	-215.88
[25]	130	3.88	37.42	-138.00	3	13.60	-200.35
[26]	130	13.93	13.29	-100.60	1	0.60	-188.16
[27]	130	4.90	2.50	-135.70	3	3.00	-183.15
[28]	130	8.58	15.51	-106.20	1	4.00	-182.66
[29]	130	13.75	10.91	-104.60	1	5.00	-181.13
[30]	130	19.48	4.88	-103.00	1	5.00	-175.56
[31]	130	6.00	5.33	-115.00	1	12.50	-174.13

Table 2. Common VCO Performance Metrics

1.3 Down conversion mixer

A down conversion mixer was designed using a Gilbert cell. In the same structure as the up conversion mixer, the circuit for frequency conversion was made as follows.

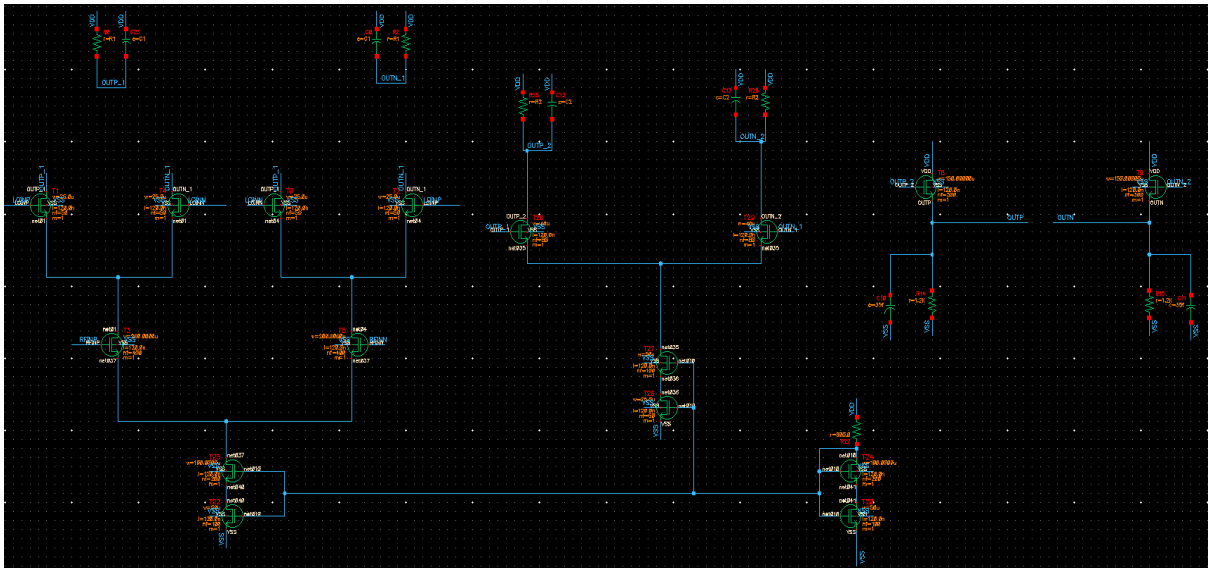


Figure 7. Down conversion mixer Circuit

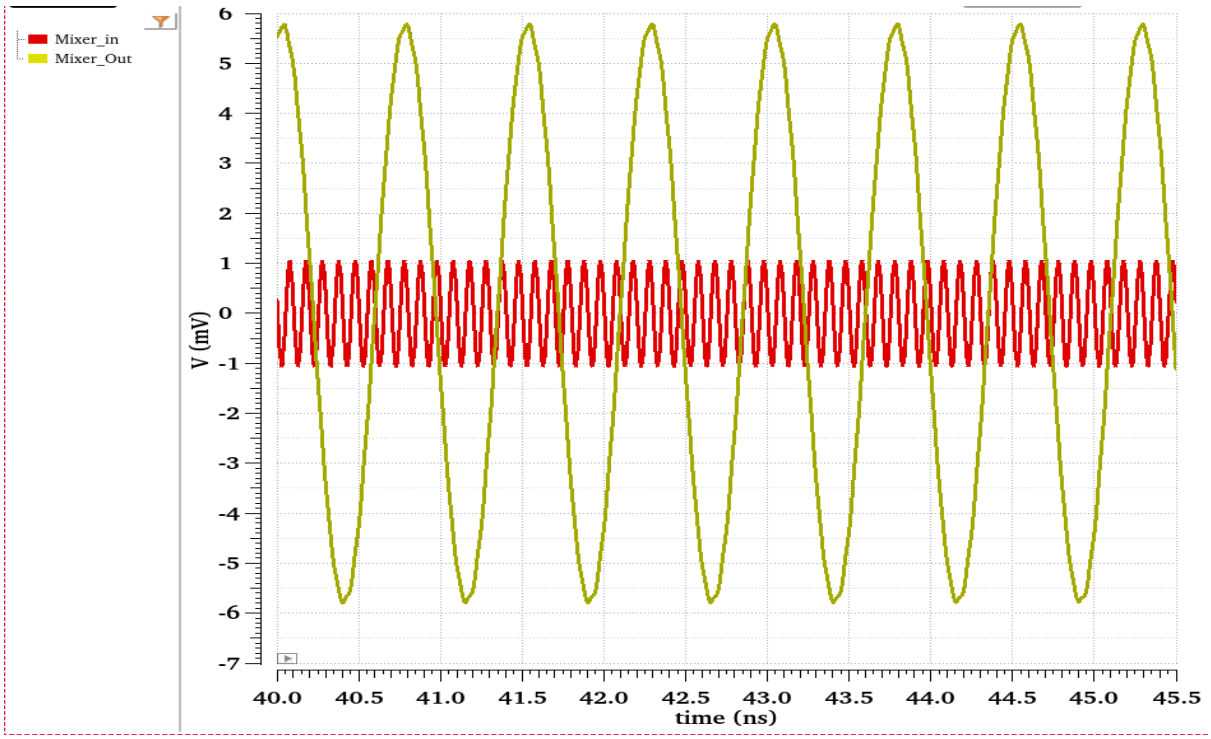


Figure 8. Mixer Simulation

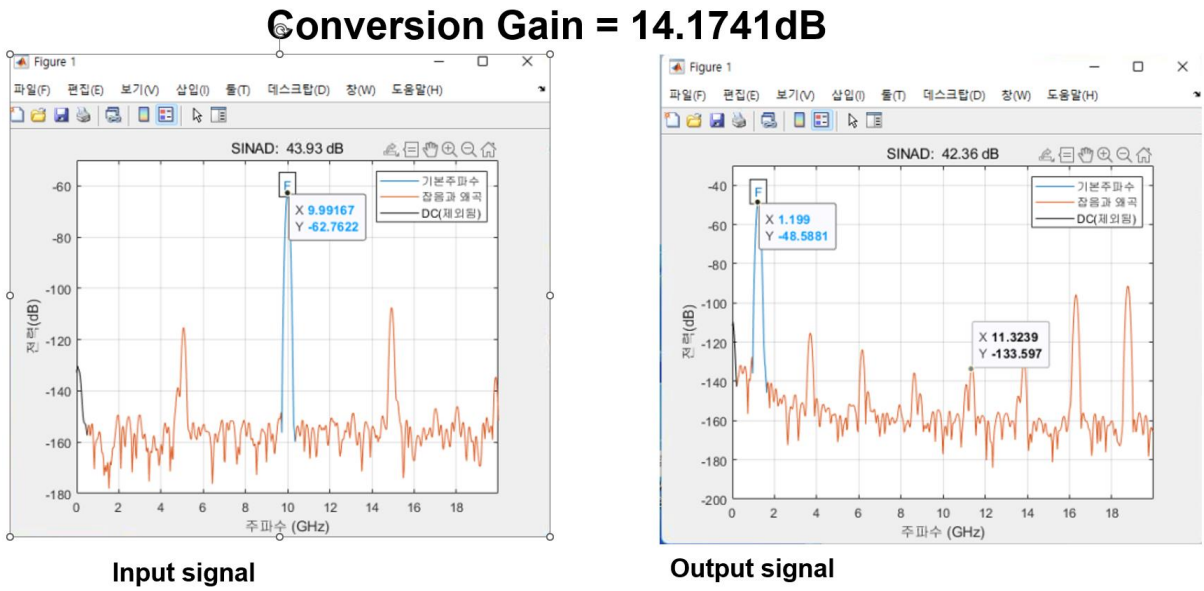


Figure 9. Conversion Gain of mixer

2. Transmitter

To design circuits for write operation. The overall goal is to design and optimize circuits for fast write operation with minimized power consumption.

System

Design X-Band Transmitter widely used in communication channels.

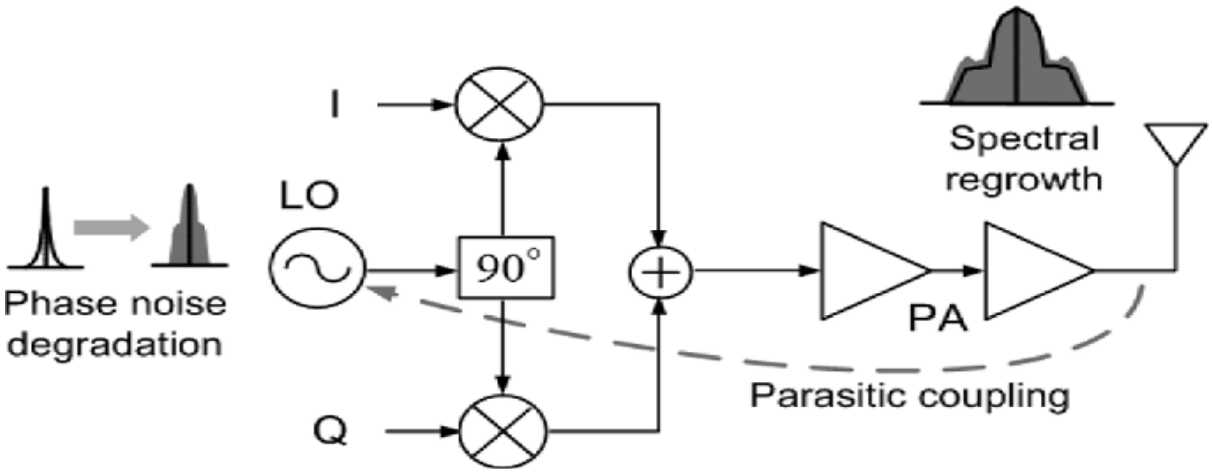


Figure 10. Transmitter Configuration

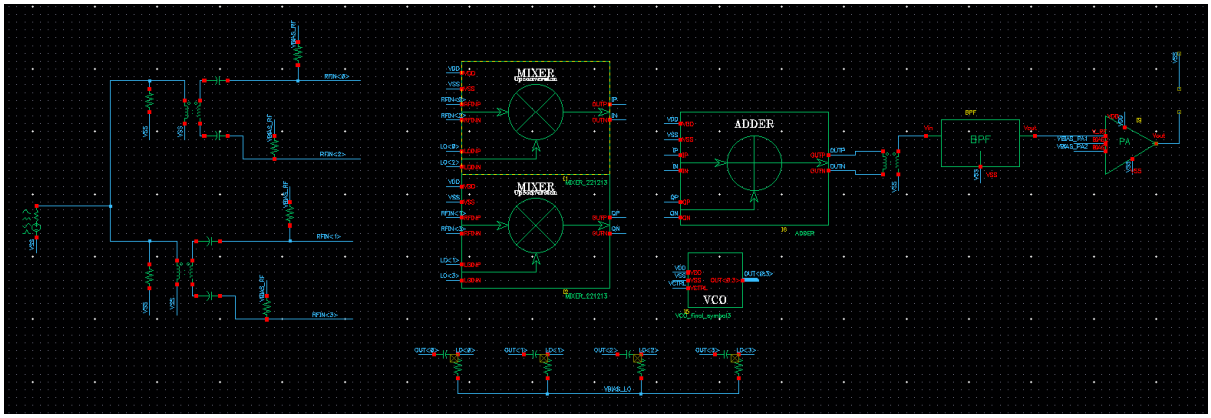


Figure 11. Transmitter schematic

2.1 Power amplifier

First of all, it is important how much power is amplified because electromagnetic waves can reach a desired destination when a signal is emitted from an antenna with appropriate maximum power in the transmitter. The PA, the last circuit before output in the transmitter, needs to step up the power by taking a relatively strong signal with a very high SNR from the network. All common factors for a signal are known, such as amplitude, modulation, shape, and duty cycle. The basic parameter of a power amplifier is the output power at the frequency of interest, and typically the gain of a PA is 10dB to 30dB. Efficiency, along with gain, is an important parameter, and the efficiency of a PA is typically between 30% and 80%, but it depends on so many factors. PAs, like LNAs, are also critical for linearity and are rated via IP3. Also, gain and efficiency are checked, and efficiency is checked through power added efficiency.

Power amplifiers include class A, class AB, and class B amplifiers. PAE is class A amplifier: 25% or 50%, class AB amplifier: 25~78.5%, class B amplifier: 78.5%. The class A amplifier outputs the same input waveform, and the class AB amplifier and

the class B amplifier are difficult to reproduce in the same way.

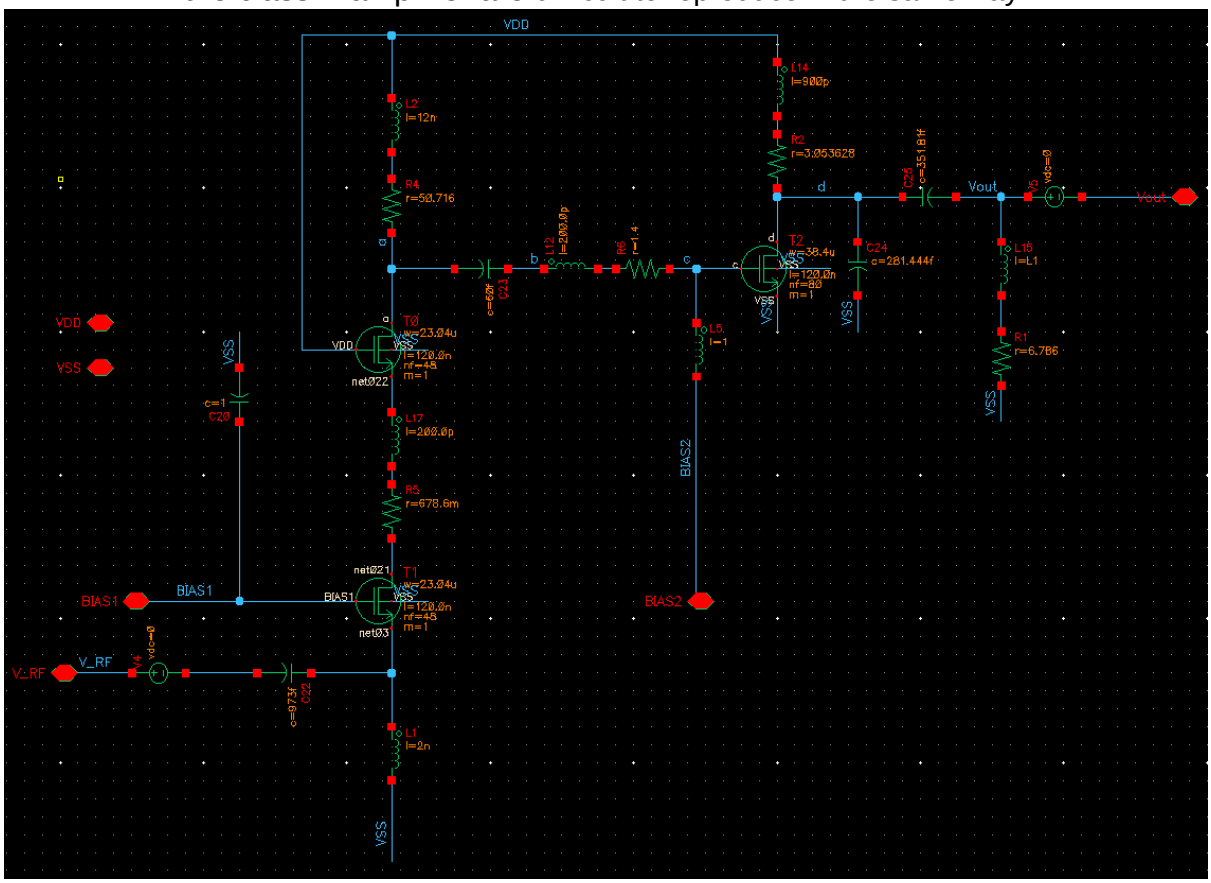


Figure 12. Proposed Power amplifier

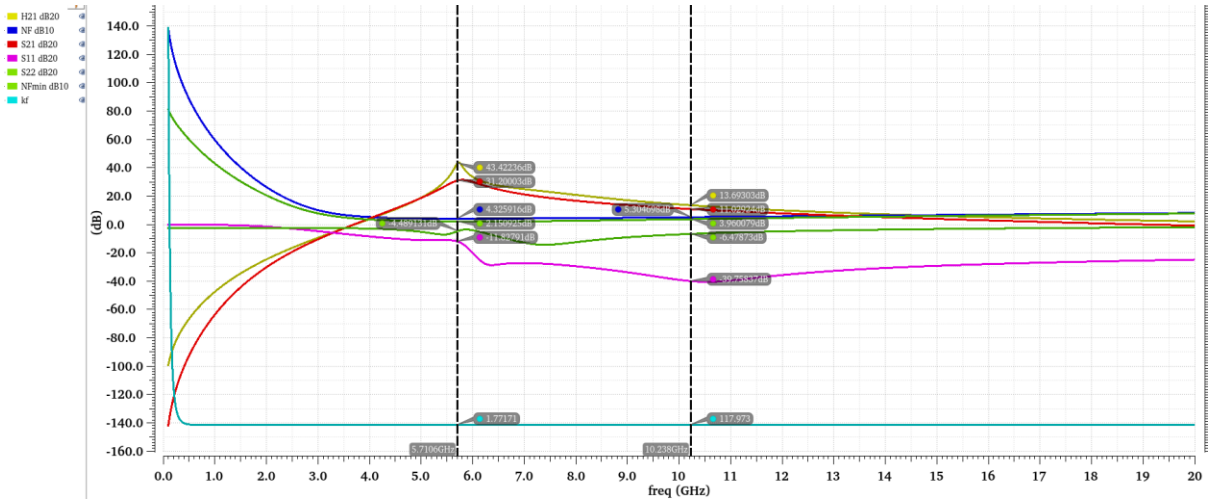


Figure 13. PA S-parameter & Gain

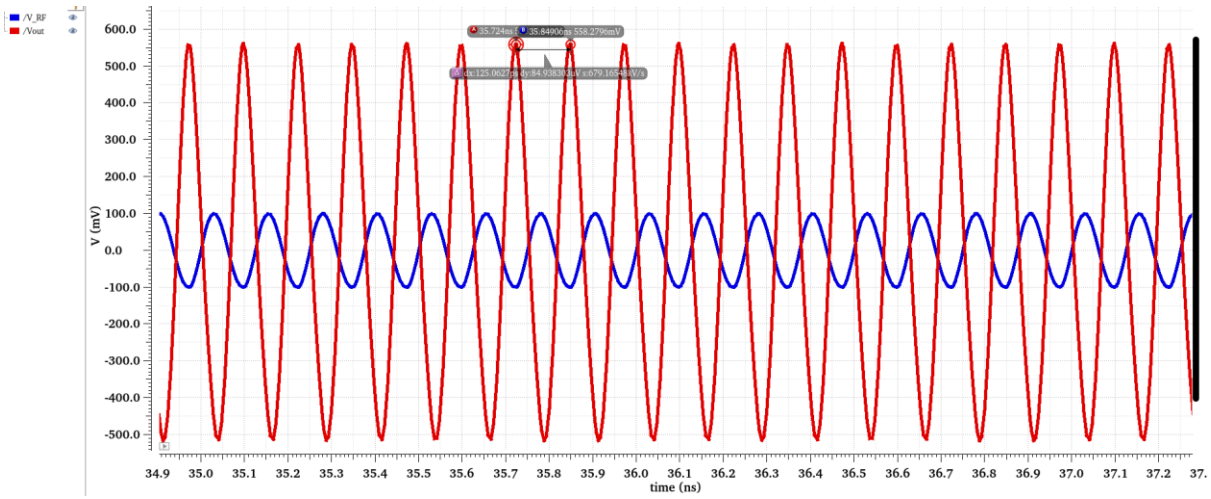


Figure 14. PA Input & Output voltage

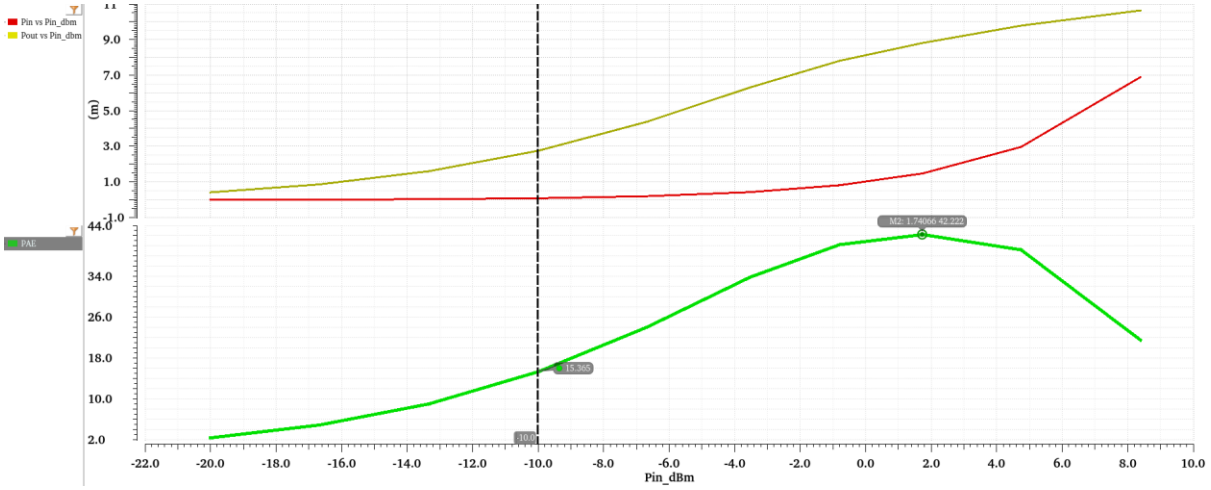


Figure 15. Power amplifier PAE (Green line)

PA Design

Power Amplifier is designed using CG-stage, and impedance matching is performed through L1 inductor, C22 capacitor and gm value. Also CG amp. It is easy to properly match the target uwb transceiver because it has wide band characteristics. I connected the cs amplifier of the output to raise the insufficient gain. Therefore, the gain at the target frequency is 11dB ~ 29dB, and the NF is 4.3dB ~ 5.3dB. As with the PA characteristics, the current gain was obtained up to 13dB ~ 40dB, which is slightly higher than the gain. However, although it was supposed to show 25% characteristics in PAE, the above result, which was different from the expected PAE, was obtained due to the reason that the linearity fluctuated, including the fact that the output waveform of the PA was not the same as the input waveform when the power was higher than 0dBm.

2.2 Up conversion mixer

Up conversion mixer is a circuit that converts frequency like down conversion mixer. There are several passive and active mixer structures that improve isolation, and among them, the Double Balanced Mixer (DBM) structure was used in the active mixer. Although this has a problem of complexity and size increase, it has the best isolation and harmonic cancellation characteristics.

That is, the advantages of this structure are:

Isolation between each port is greatly improved.

It can suppress the generation of various spurious or harmonic.

The use of external filters can be reduced.

The processing power limit is raised.

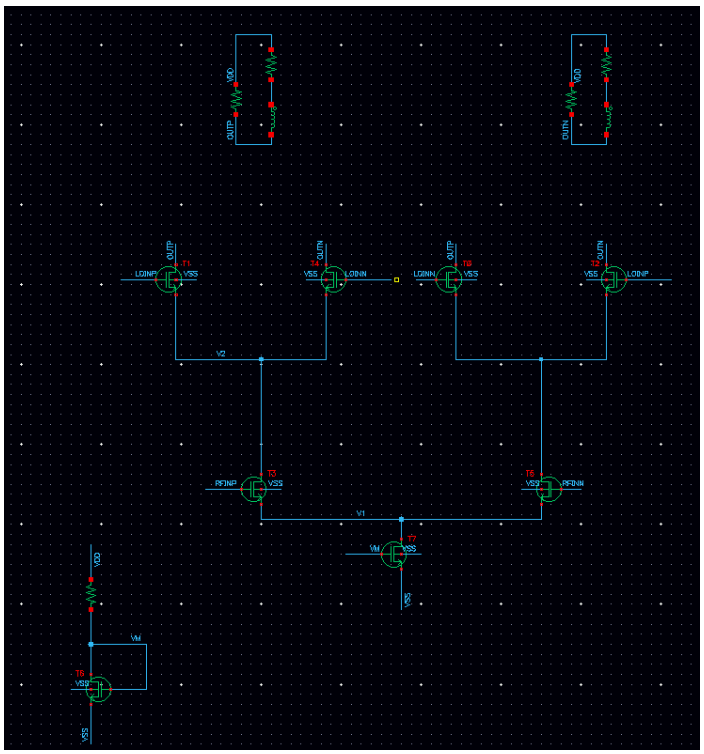


Figure 16. Up conversion mixer schematic

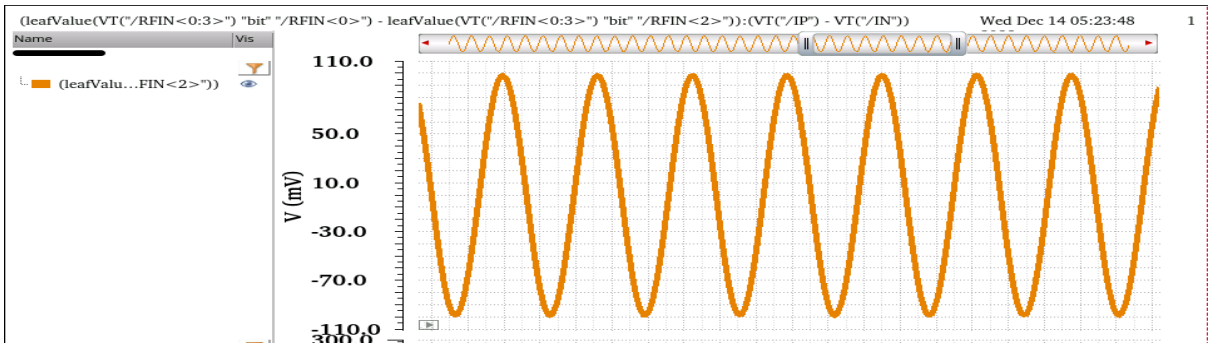


Figure 17. Output voltage of Up conversion mixer

2.3 Adder

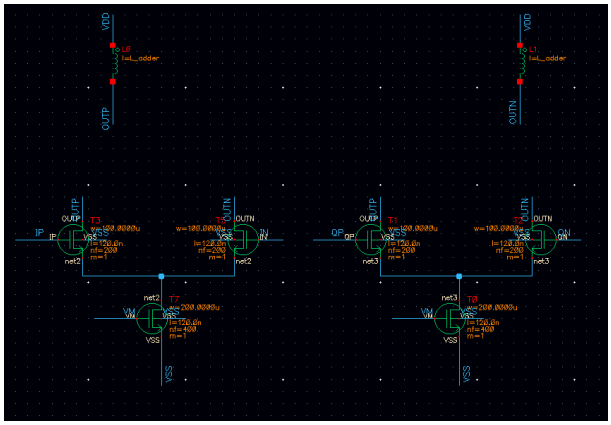
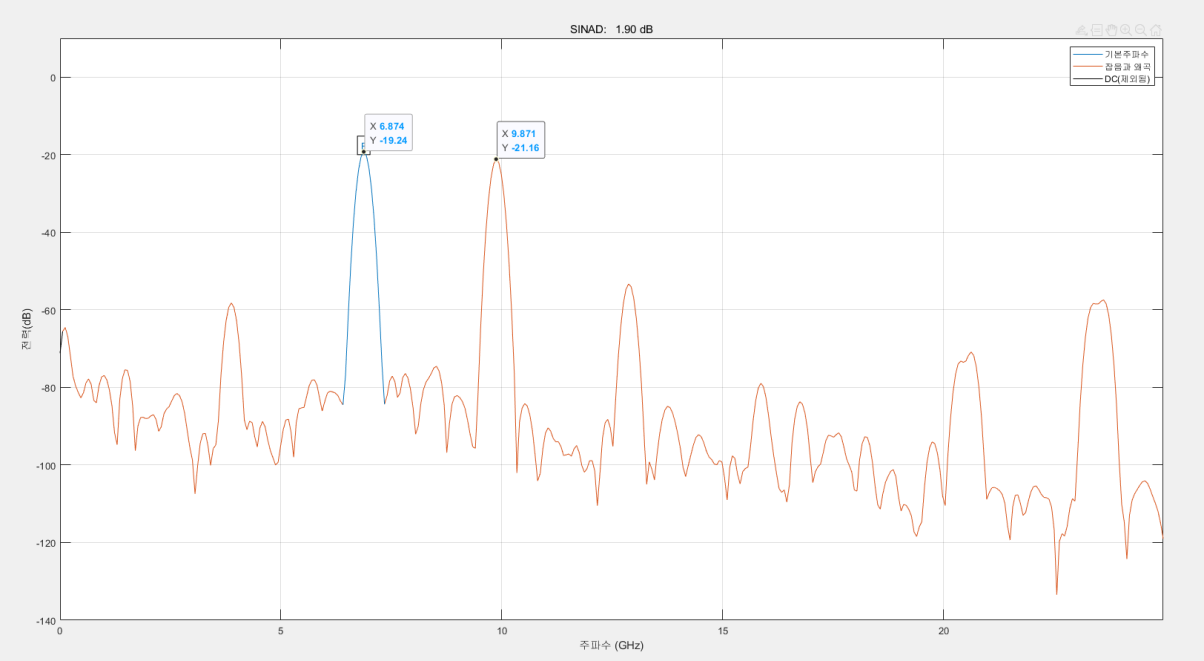


Figure 18. Adder schematic



Figuer 19. Output of Adder

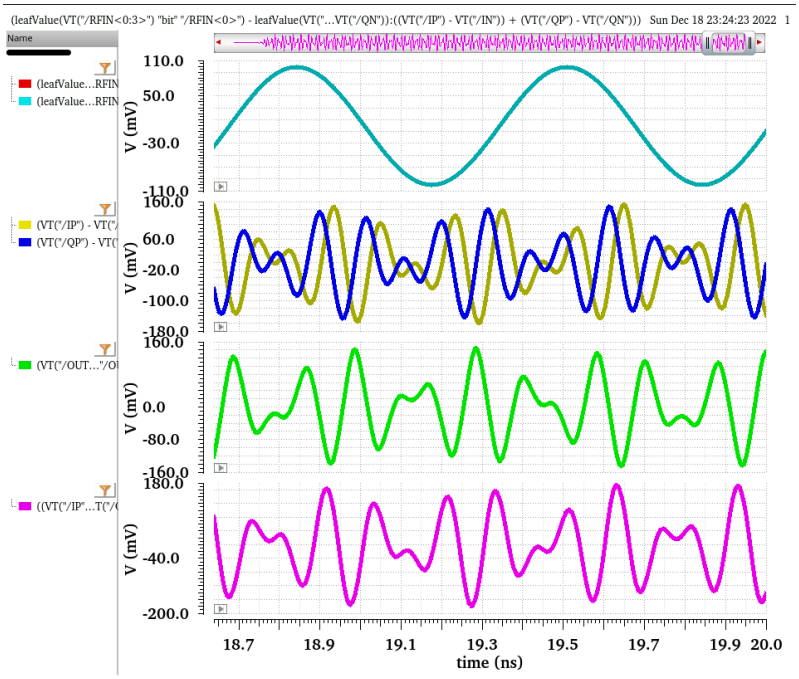


Figure 20. Output voltage of Adder

3. Conclusion

From all the work of read-path and write-path design, including charge pump and LDO circuits results in more stable read or write currents, leading to higher reliability of the designed integrated circuits.

4. Contribution

Contribution rate:

Name	김태영	김현석
Percentage	50 %	50 %